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EXAMINER	
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2892	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/766,053	HAUPT, MORITZ	
	Examiner	Art Unit	
	THANH Y. TRAN	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 7, 9, 14, and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. 6,759,335) in view of Stamp et al. (U.S. 2004/0084149).

As to claim 1, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, the method comprising: forming a trench having vertical sidewalls and a bottom formed within the substrate (10), the sidewalls and bottom of the trench being formed of the substrate material (material of substrate 10 / "semiconductor" material of 10, see col. 2, line 56); forming a vertical silicon layer ("polysilicon" 62), the silicon layer (62) not having a continuous crystalline structure; and performing gas phase doping (65) upon the exposed surface of 62 so that the silicon layer ("polysilicon" 62) is doped with a dopant having a concentration of at least 1E19 atoms/cm3 ("1E18 to 1E21 ions/cm3") (see col. 3, line 40 – col. 4, line 25).

Lee does not disclose a silicon layer having a bottom surface extending conformally over the sidewalls of the trench to continuously cover at least a lower portion of the sidewalls and the bottom of the trench, the vertical silicon layer having an exposed surface opposite the bottom surface, the exposed surface having a vertical portion substantially parallel to the sidewalls of the trench.

Stamp et al. disclose in fig. 4A a semiconductor device comprising: a silicon layer (silicon film" 410) having a bottom surface extending conformally over the sidewalls of the trench to continuously cover at least a lower portion of the sidewalls (as indicated at 460) and the bottom (as indicated at 430) of the trench, the vertical silicon layer 410 having an exposed surface (top surface of 410) opposite the bottom surface 430, the exposed surface (top surface of 410) having a vertical portion substantially parallel to the sidewalls (as indicated at 460) of the trench. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the device of Lee by comprising a silicon layer having a bottom surface extending conformally over the sidewalls of the trench to continuously cover at least a lower portion of the sidewalls and the bottom of the trench, the vertical silicon layer having an exposed surface opposite the bottom surface and the exposed surface having a vertical portion substantially parallel to the sidewalls of the trench as taught by Stamp et al. for providing good step coverage over the trench in semiconductor substrate (see para. [0061]).

As to claims 2-3, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, wherein the silicon layer (62) comprises polysilicon (62) (see col. 4, lines 8-25).

As to claim 4, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, wherein the silicon layer ("polysilicon" 62) is at least 8 nm thick ("about 20 and 100 nm") (see col. 4, lines 17-25).

As to claims 7 and 9, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, wherein the dopant is arsenic or phosphorous (see col. 4, lines 8-16).

As to claim 14, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, wherein forming the silicon layer ("polysilicon" 62) and performing the gas phase doping (65) comprise an in-situ process (see col. 4, lines 8-16).

As to claim 16, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, further comprising: performing a wet clean ("wet process") of the substrate before performing the gas phase doping (65), wherein the wet clean ("wet process") removes a native oxide on the silicon layer (see figures 4-7, and col. 3, lines 37-39).

As to claim 17, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, further comprising substantially filling the trench with a fill material (64) after performing the gas phase doping (65) (see figures 7-8), wherein a lower surface of the fill material (64) is disposed on the exposed surface (top surface of 62).

3. Claims 5-6, 8, 10-13 and 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. 6,759,335) in view Stamp et al. (U.S. 2004/0084149) as applied to claims 1 and 18 above, and further in view of Chung et al (U.S. 6,734,106).

As to claims 5, 6, 8, 10, 11, 12, and 13, Lee in view of Stamp et al. does not disclose the gas phase doping is performed at a temperature between about 850-1000° C or a temperature between 850-950° C; the gas phase doping is performed at a pressure of between 1-100 Torr; the gas phase doping uses AsH.sub.3 as a dopant precursor or dopant is arsenic formed by an AsH.sub.3 precursor; the precursor is flowed at a rate of 100-300 sccm for between 5-120 minutes.

Chung et al discloses in col. 2, line 49 - col. 3, line 20, a method wherein the gas phase doping is performed at a temperature between about 850-1000° C ("about 900 to 1000° C") or a temperature between 850-950 ° C ("about 900 to 1000° C"); the gas phase doping is performed at a pressure of between 1-100 Torr ("about 100 torr"); the gas phase doping uses AsH.sub.3 ("AsH3") as a dopant precursor or dopant is arsenic formed by an AsH.sub.3 ("AsH3") precursor; the precursor is flowed at a rate of 100-300 sccm ("about 200") for between 5-120 minutes ("about 120 … minutes"). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Lee in view of Stamp et al. by having the gas phase doping which is performed at a temperature between about 850-1000° C or a temperature between 850-950 ° C; the gas phase doping is performed at a pressure of between 1-100 Torr; the gas phase doping uses AsH.sub.3 as a dopant precursor or dopant is arsenic formed by an AsH.sub.3 precursor; the precursor is flowed at a rate of 100-300 sccm for between 5-120 minutes as taught by Chung et al for protecting the upper surface of the substrate.

Lee in view of Stamp et al. and Chung does not disclose the step of forming the silicon layer is performed at a temperature less than the gas phase doping; and the gas phase doping is performed at a pressure of between 15-30 Torr. However, the temperature range for the silicon layer; and the pressure range for the gas phase doping would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of

any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Lee in view of Stamp et al. and Chung does not disclose the precursor is flowed in the presence of H2 or He. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Lee in view of Stamp et al. and Chung by using H2 or He material for flowing the precursor for controlling the rate and processing time of the precursor, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended used as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

As to claim 18, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, the method comprising: forming a trench having vertical sidewalls and a bottom within the substrate (10), the sidewalls and the bottom of the trench being formed of the substrate material (material of substrate 10 / "semiconductor" material of 10, see col. 2, line 56); lining the sidewalls with a node dielectric (20) and forming sidewalls of the node dielectric (20); depositing a silicon layer ("polysilicon" 62) and a top surface of the node dielectric (20) (see figures 6-7, the end portion of 62 having a first surface in contact with 20), the silicon layer (62) not having a continuous crystalline structure; wherein the gas phase doping (65) results in the silicon layer ("polysilicon" 62) being doped with a dopant having a concentration of at least 1E19 atoms/cm.sup.3 ("1E18 to 1E21 ions/cm3") (see col. 3, line 40 – col. 4, line 25).

Lee does not disclose a silicon layer having a bottom surface in contact with and continuously and conformally covering at least a lower portion of the sidewalls, the silicon layer having an exposed surface opposite the bottom surface, the exposed surface having a vertical portion substantially parallel to the sidewalls of the trench.

Stamp et al. disclose in fig. 4A a semiconductor device comprising: a silicon layer (silicon film" 410) having a bottom surface in contact with and continuously and conformally covering at least a lower portion of the sidewalls (as indicated at 460), the silicon layer 410 having an exposed surface (top surface of 410) opposite the bottom surface 430, the exposed surface (top surface of 410) having a vertical portion substantially parallel to the sidewalls (as indicated at 460) of the trench. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the device of Lee by comprising a silicon layer having a bottom surface in contact with and continuously and conformally covering at least a lower portion of the sidewalls, the silicon layer having an exposed surface opposite the bottom surface, the exposed surface having a vertical portion substantially parallel to the sidewalls of the trench as taught by Stamp et al. for providing good step coverage over the trench in semiconductor substrate (see para. [0061]).

Lee in view of Stamp et al. does not disclose a method comprising: performing gas phase doping in a reaction chamber by: flowing a dopant precursor gas in the reaction chamber at a rate of between 100-300 sccm, heating the reaction chamber to a temperature of between 850-1000 degree C, and pressurizing the reaction chamber to a pressure of between 1-100 Torr.

Chung et al discloses in col. 2, line 49 - col. 3, line 20, a method comprising: performing gas phase doping in a reaction chamber by: flowing a dopant precursor gas in the reaction

chamber at a rate of between 100-300 sccm ("about 200"), heating the reaction chamber to a temperature of between 850-1000 degree C ("about 900 to 1000° C"), and pressurizing the reaction chamber to a pressure of between 1-100 Torr ("about 100 torr") for protecting the upper surface of the substrate. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Lee in view of Stamp et al. by having the step of performing gas phase doping in a reaction chamber by: flowing a dopant precursor gas in the reaction chamber at a rate of between 100-300 sccm, heating the reaction chamber to a temperature of between 850-1000 degree C, and pressurizing the reaction chamber to a pressure of between 1-100 Torr as taught by Chung et al for protecting the upper surface of the substrate.

As to claim 19, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, further comprising substantially filling the trench with a fill material (64, figure 8) after performing the gas phase doping (65, figure 7), wherein a lower surface of the fill material 64 is disposed on the exposed surface (top surface of 62).

As to claims 20-21, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, wherein the silicon layer ("polysilicon" 62) comprises polysilicon (see col. 4, lines 8-25).

As to claim 22, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, wherein the silicon layer ("polysilicon" 62) is at least 8 nm thick ("about 20 and 100 nm") (see col. 4, lines 17-25).

As to claim 23, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, wherein the dopant is arsenic or phosphorous (see col. 4, lines 8-16).

As to claim 24, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, wherein forming the silicon layer ("polysilicon" 62) and performing the gas phase doping (65) comprise an in-situ process (see col. 4, lines 8-16).

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. 6,759,335) in view Stamp et al. (U.S. 2004/0084149) as applied to claim 1 above, and further in view of Cheong (U.S. 2003/0186533).

As to claim 15, Lee in view Stamp et al. does not disclose a method wherein forming the silicon layer and performing the gas phase doping comprise an ex-situ process.

Cheong discloses in paragraphs [0005] and [0029] a method, wherein forming the silicon layer ("silicon thin film") and performing the gas phase doping comprise an ex-situ process. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Lee in view Stamp et al. by having the steps of forming the silicon layer and performing the gas phase doping comprise an ex-situ process as taught by Cheong for removing contaminants which are produced by such contaminator as carbon and oxides (see paragraph [0029] in Cheong).

5. Claims 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. 6,759,335) in view Stamp et al. (U.S. 2004/0084149) and Chung et al (U.S. 6,734,106) as applied to claim and 18 above, and further in view of Cheong (U.S. 2003/0186533).

As to claim 25, Lee in view of Stamp et al. and Chung et al. does not disclose a method wherein forming the silicon layer and performing the gas phase doping comprise an ex-situ process.

Cheong discloses in paragraphs [0005] and [0029] a method, wherein forming the silicon layer ("silicon thin film") and performing the gas phase doping comprise an ex-situ process. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Lee in view of Stamp et al. and Chung et al. by having the steps of forming the silicon layer and performing the gas phase doping comprise an ex-situ process as taught by Cheong for removing contaminants which are produced by such contaminator as carbon and oxides (see paragraph [0029] in Cheong).

As to claim 26, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, further comprising: performing a wet clean ("wet process") of the substrate (figure 4) before performing the gas phase doping (65) (figure 6), wherein the wet clean ("wet process") removes a native oxide on the silicon layer ("polysilicon" 62).

As to claim 27, Lee in view of Stamp et al. and Chung et al. does not disclose a method wherein the dopant has a concentration of at least 5x10.sup.19 atoms/cm.sup.3.

Cheong discloses in col. 4, lines 57-59 a method, wherein the dopant has a concentration of at least 5x10.sup.19 atoms/cm.sup.3 ("about 1x10.sup.19 atoms/cm.sup.3 to about 21x10.sup.20 atoms/cm.sup.3"). Applicant should note that: 5x10.sup.19 atoms/cm.sup.3 falls in the range of "about 1x10.sup.19 atoms/cm.sup.3 to about 21x10.sup.20 atoms/cm.sup.3" (see paragraphs [0016] & [0017]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Lee in view

of Stamp et al. and Chung et al. by having the dopant which has a concentration of at least 5x10.sup.19 atoms/cm.sup.3 as taught by Cheong for preventing outdiffusing phosphorus doped on junction area through a thermal budget according to a subsequent thermal process (see paragraph [0035] in Cheong).

6. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. 6,759,335) in view of Mo (U.S. 2002/0024091).

As to claim 29, Lee discloses in figures 5-7 a method of fabricating a semiconductor device in a substrate, the method comprising: forming a trench having sidewalls and a bottom formed within the substrate (10), the sidewalls and bottom of the trench being formed of the substrate material (material of substrate 10 / "semiconductor" material of 10, see col. 2, line 56); a silicon liner 62 having an exposed surface (top surface of 62), the silicon liner 62 not having a continuous crystalline structure; and performing gas phase doping (65) upon the exposed surfaces of the silicon liner ("polysilicon" 62) so that the silicon liner ("polysilicon" 62) is doped with a dopant having a concentration of at least 1El9 atoms/cm3 ("lE18 to 1E21 ions/cm3") (see col. 3, line 40 - col. 4, line 25).

Lee does not disclose lining the sidewalls and the bottom of the trench with a node dielectric, the node dielectric having a top surface parallel to the sidewalls and the bottom of the trench; and forming a continuous and conformal silicon liner, a bottom surface of the silicon liner covering at least a portion of the top surface of the node dielectric, the silicon liner having an exposed surface opposite the bottom surface and substantially parallel to the sidewalls and the bottom of the trench.

Mo discloses in figs. 6A-6C a semiconductor device comprising: lining the sidewalls and the bottom of the trench 602 with a node dielectric ("gate dielectric layer" 612), the node dielectric 612 having a top surface parallel to the sidewalls and the bottom of the trench 602; and forming a continuous and conformal silicon liner ("polysilicon layer" 614), a bottom surface of the silicon liner 614 covering at least a portion of the top surface of the node dielectric 614, the silicon liner 614 having an exposed surface (top surface of 614) opposite the bottom surface and substantially parallel to the sidewalls and the bottom of the trench 602. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the device of Lee by lining the sidewalls and the bottom of the trench with a node dielectric, the node dielectric having a top surface parallel to the sidewalls and the bottom of the trench; and forming a continuous and conformal silicon liner, a bottom surface of the silicon liner covering at least a portion of the top surface of the node dielectric, and the silicon liner having an exposed surface opposite the bottom surface and substantially parallel to the sidewalls and the bottom of the trench, as taught by Mo for providing good step coverage over the trench in semiconductor substrate (see para. [0061]).

Lee in view of Mo does not disclose the trench extending to a depth of about 6μm and 8 μm. However, the depth of about 6μm and 8 μm for a trench would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular

chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Response to Arguments

7. Applicant's arguments with respect to claims 1-27 and 29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to THANH Y. TRAN whose telephone number is (571)272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892

/T. Y. T./
Examiner, Art Unit 2892